

FIG. 1

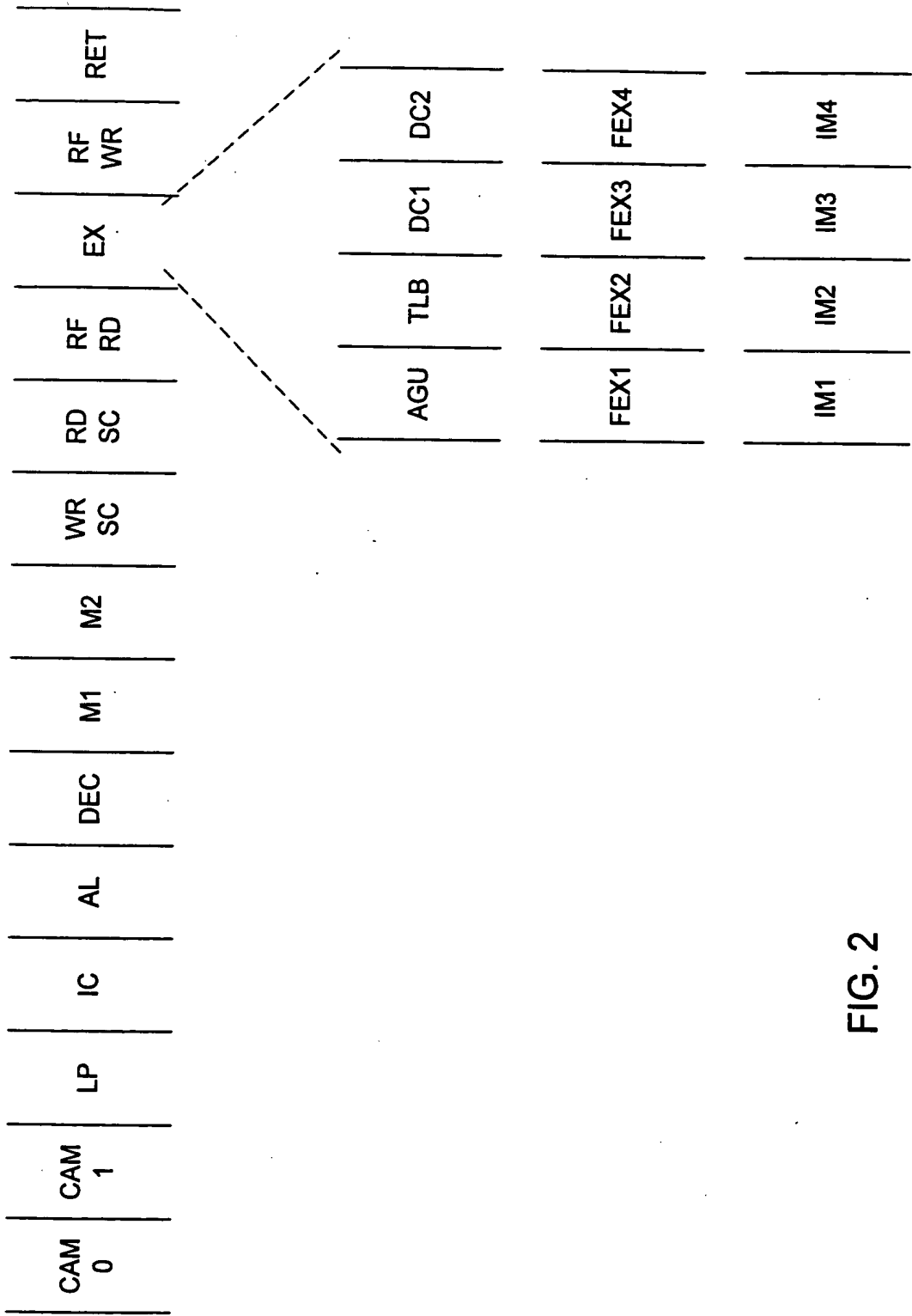


FIG. 2

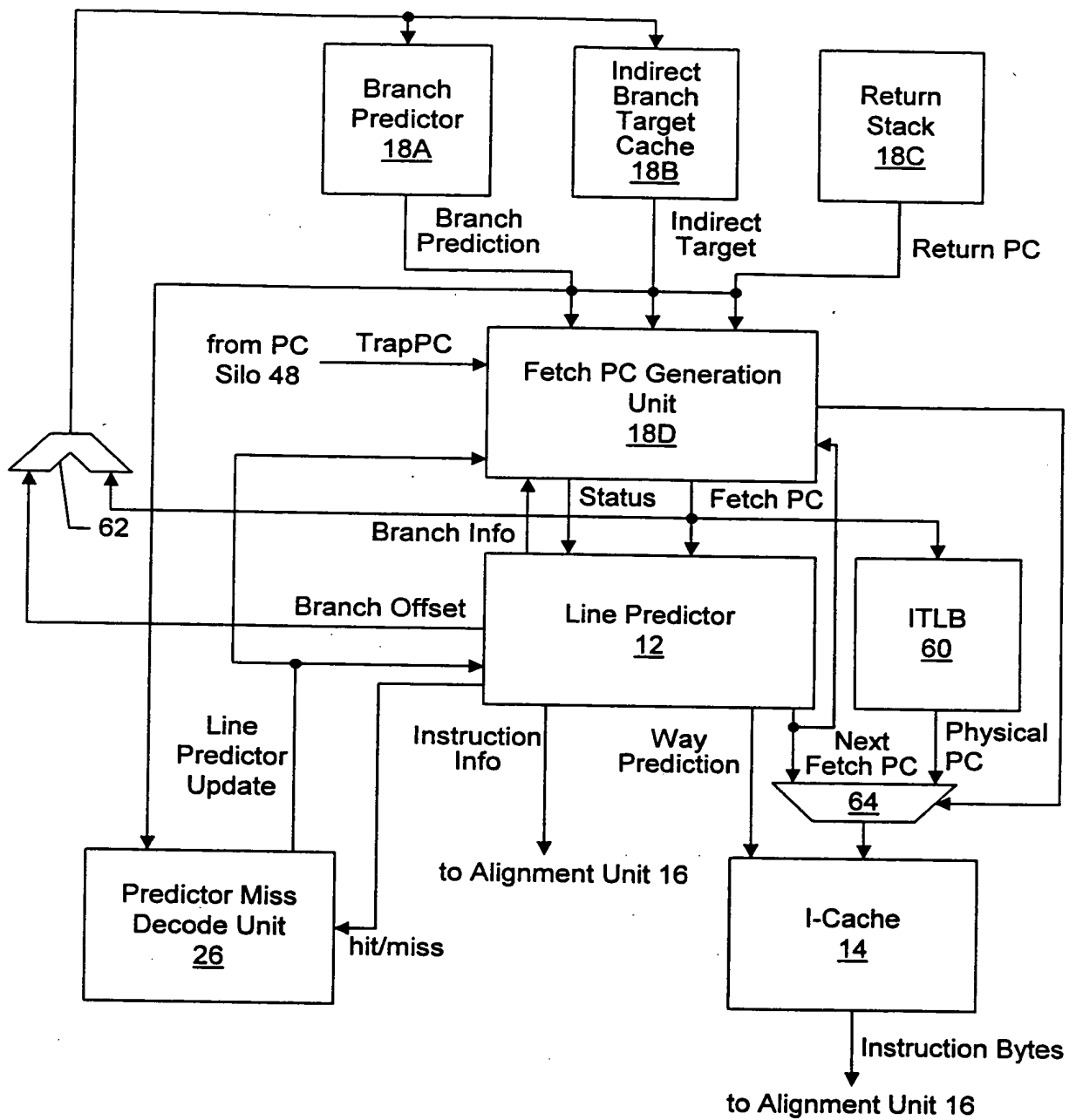


FIG. 3

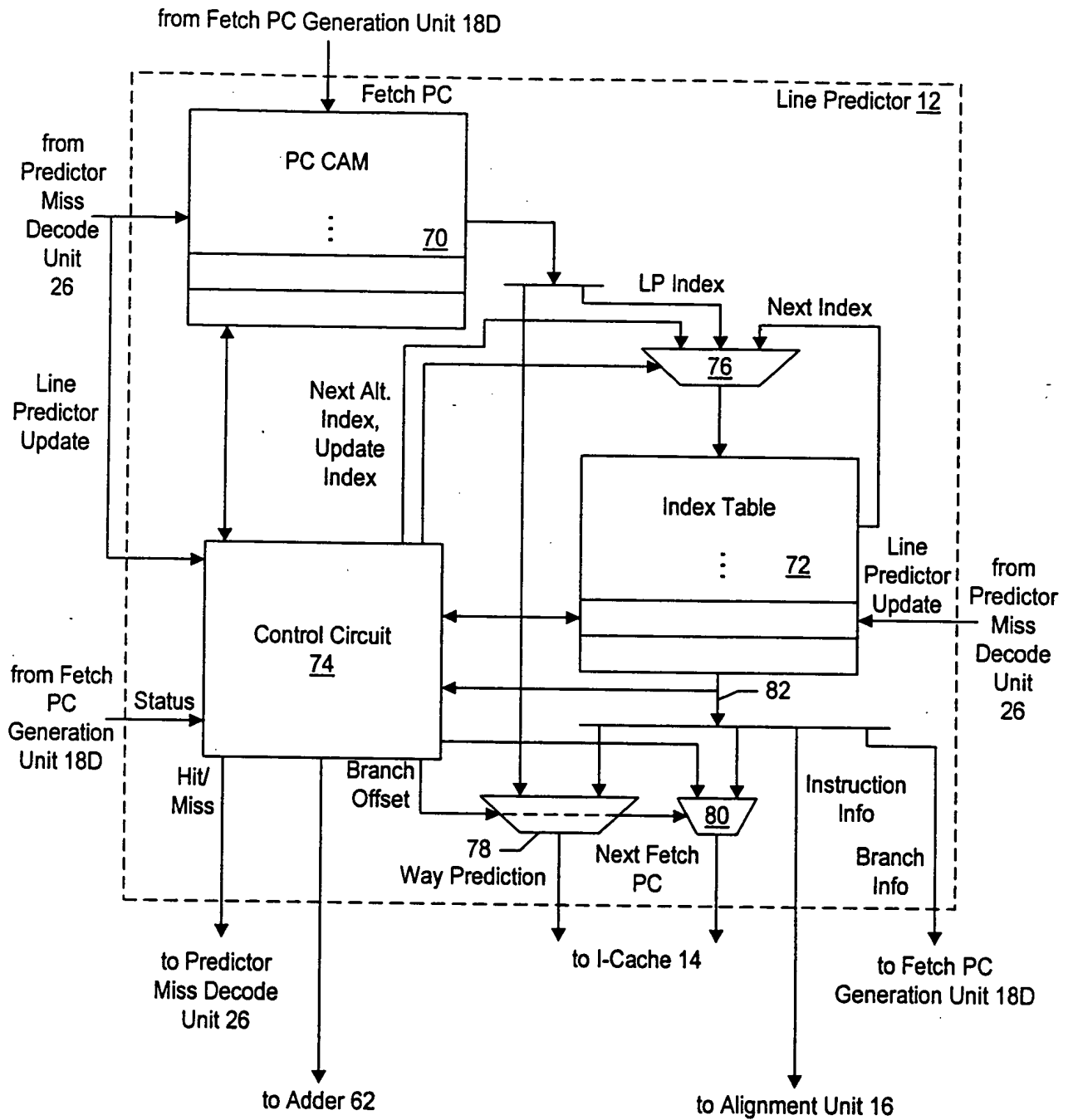


FIG. 4

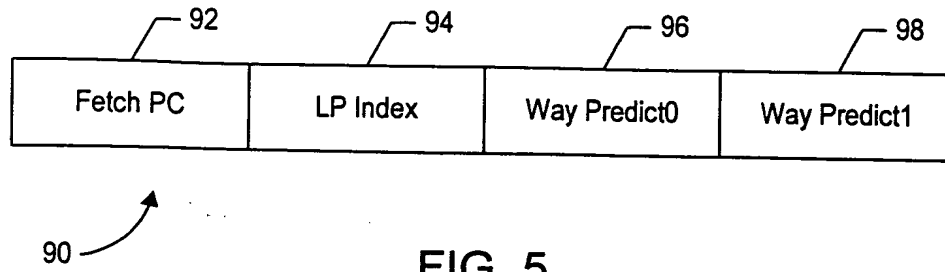


FIG. 5

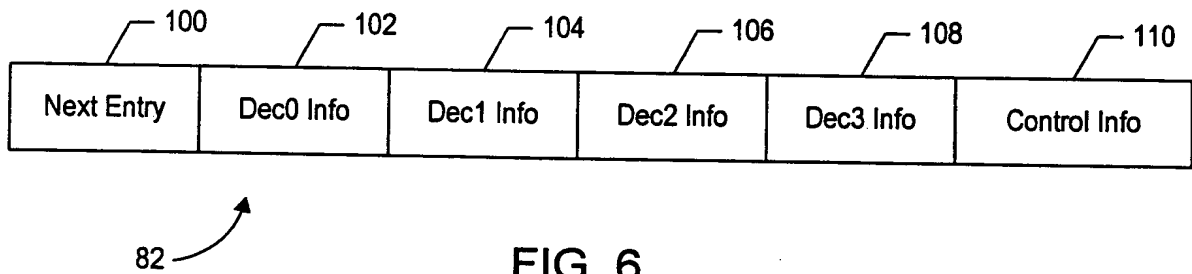


FIG. 6

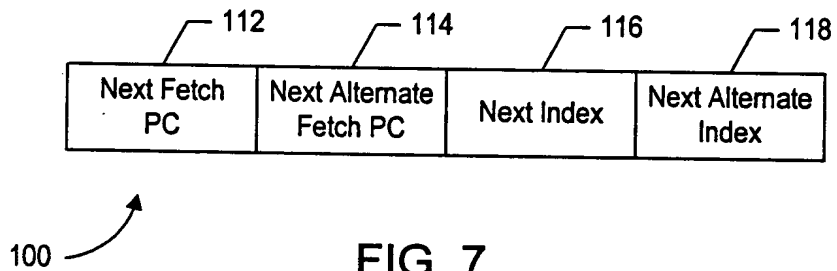


FIG. 7

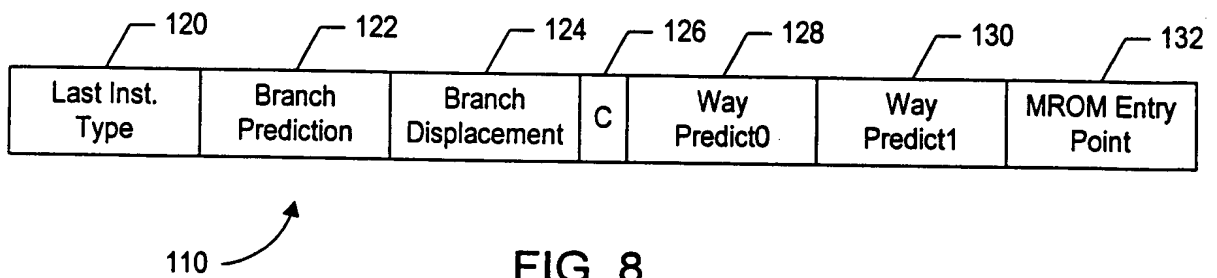


FIG. 8

<u>Line Termination Conditions</u>
Microcode Instruction
Branch Instruction
Maximum # of Instructions
Maximum # of Instruction Bytes
Maximum # of ROPs
Page Crossing
Maximum Number of Destination Registers (Maximum Number of Renames)


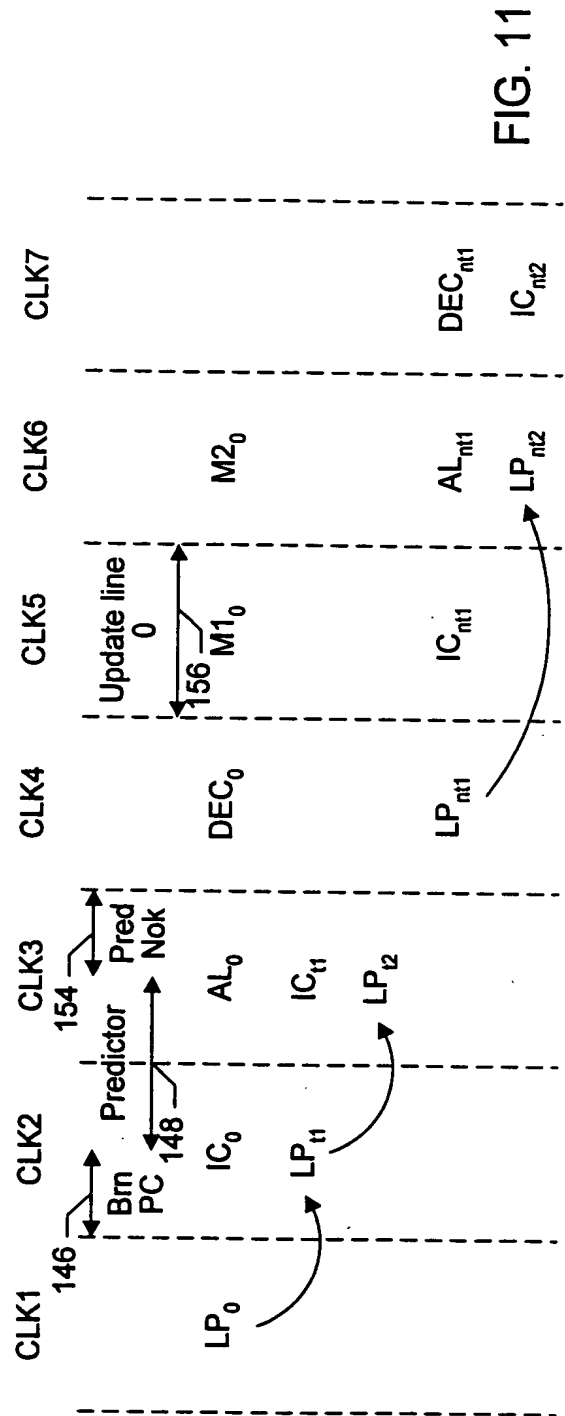
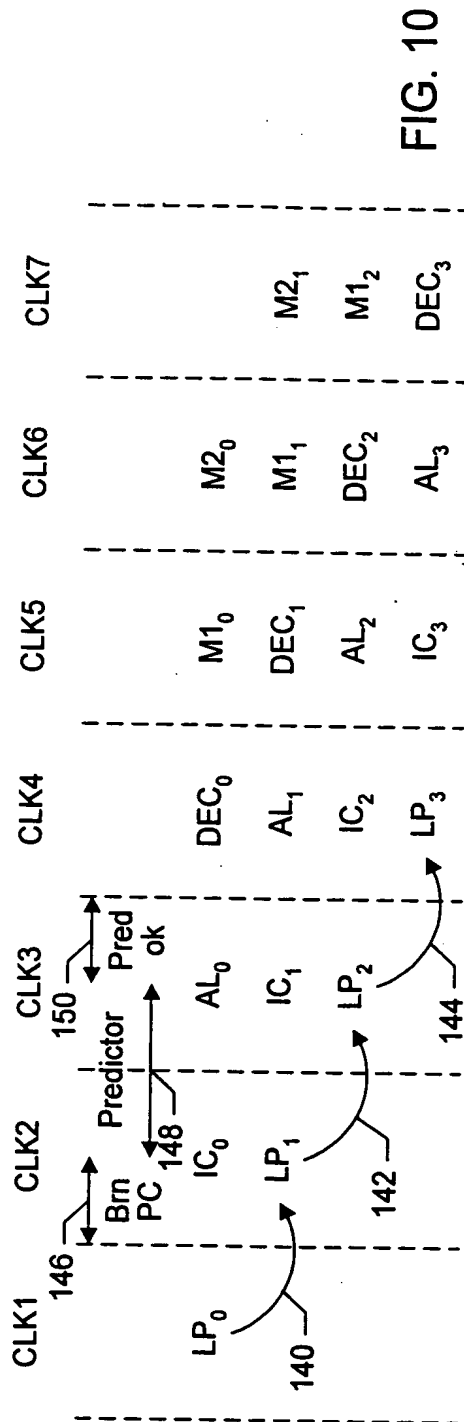
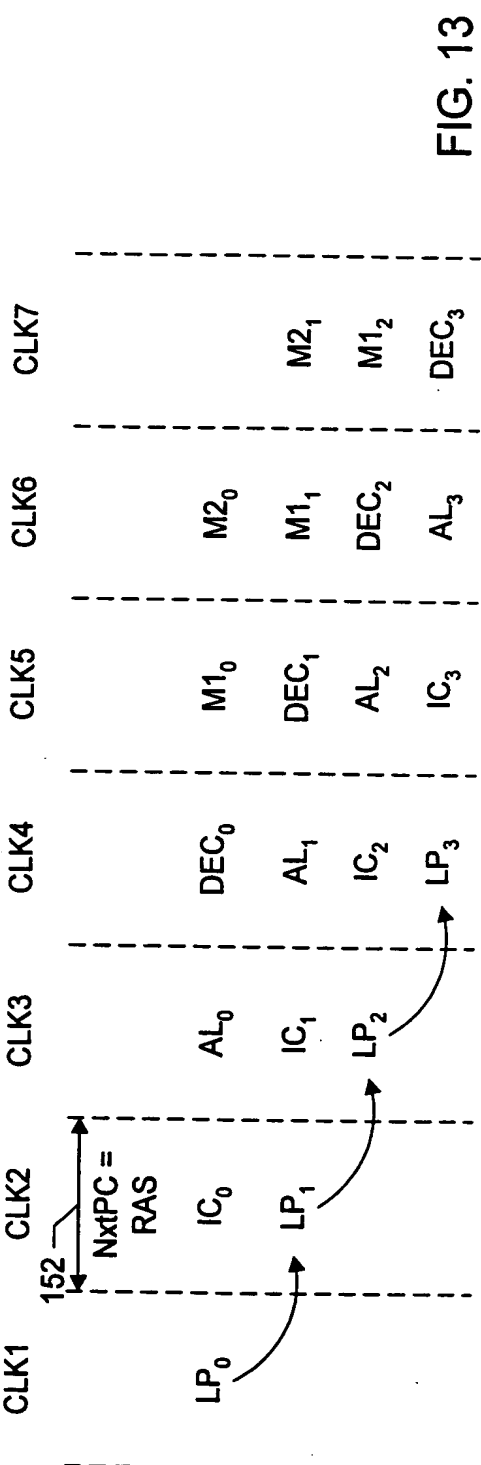
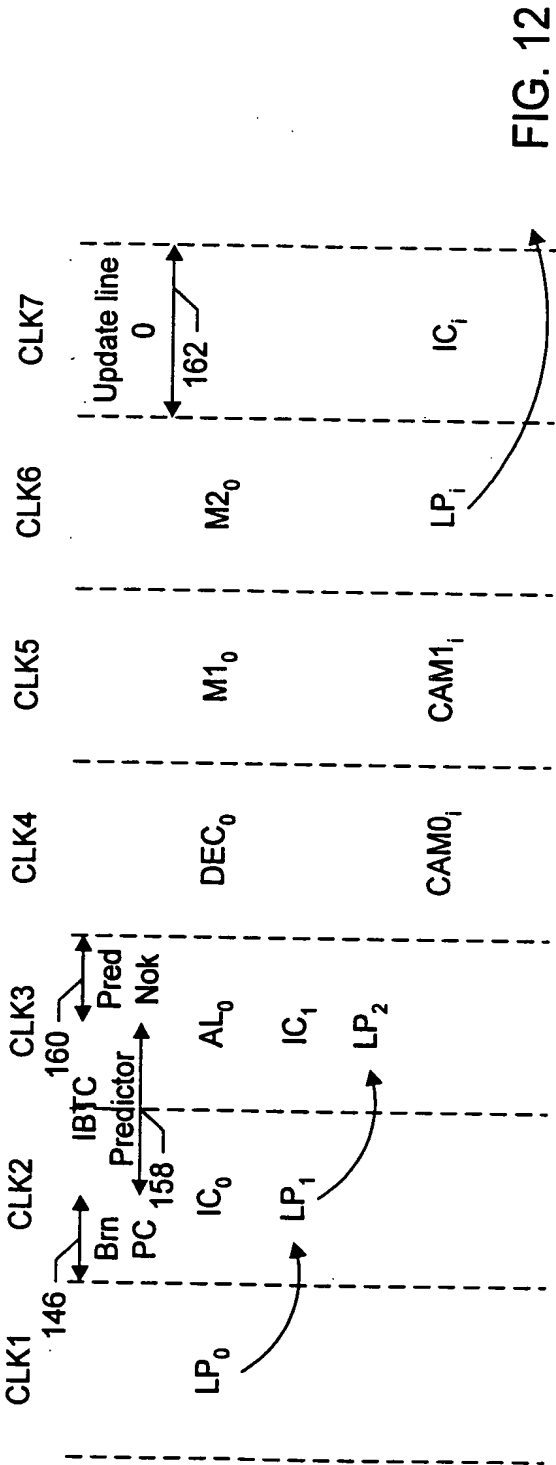
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FIG. 9





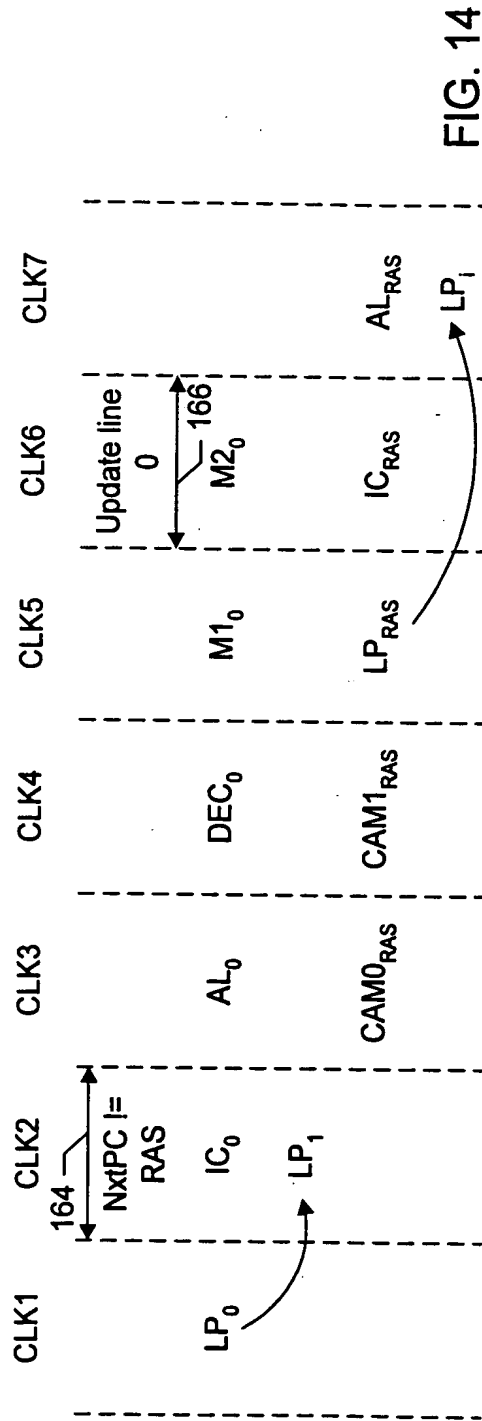


FIG. 14

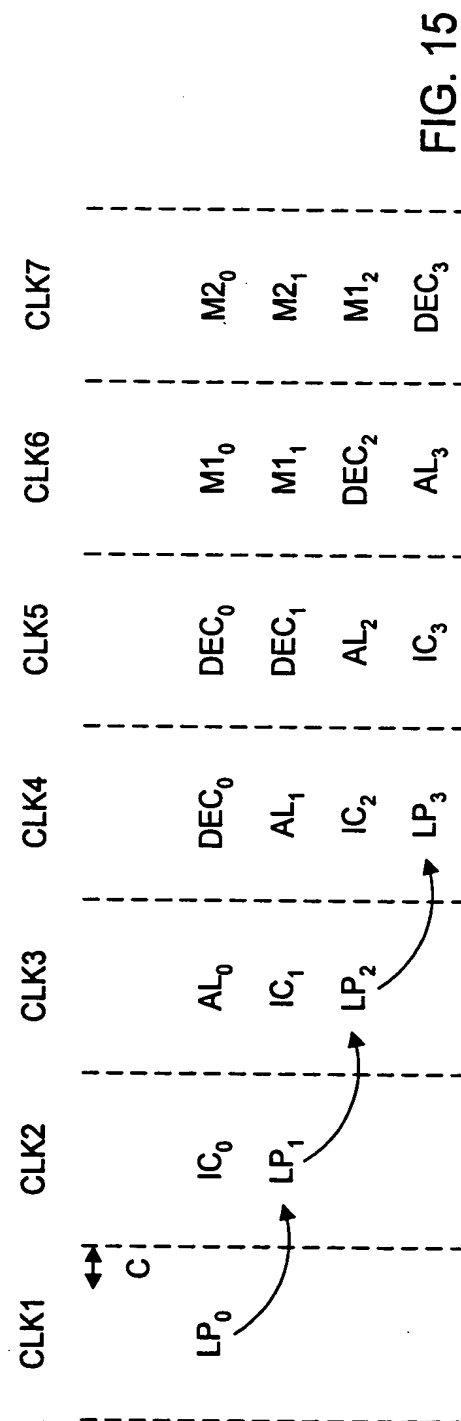
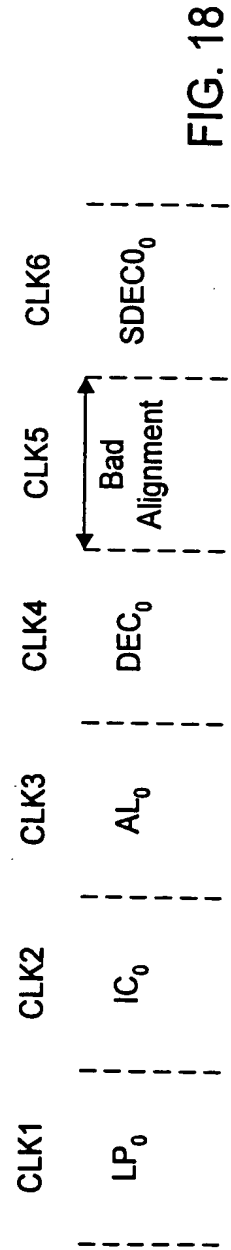
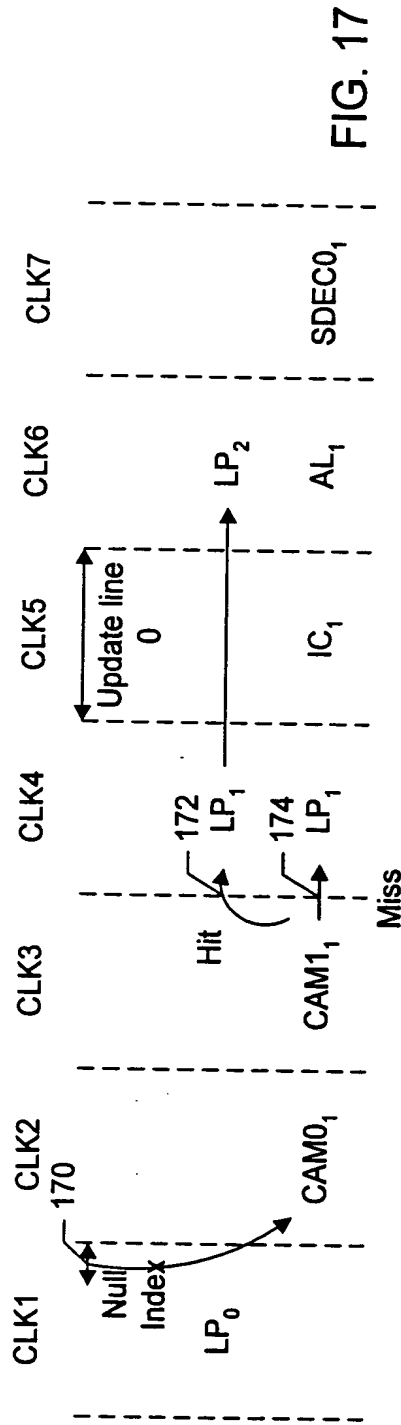
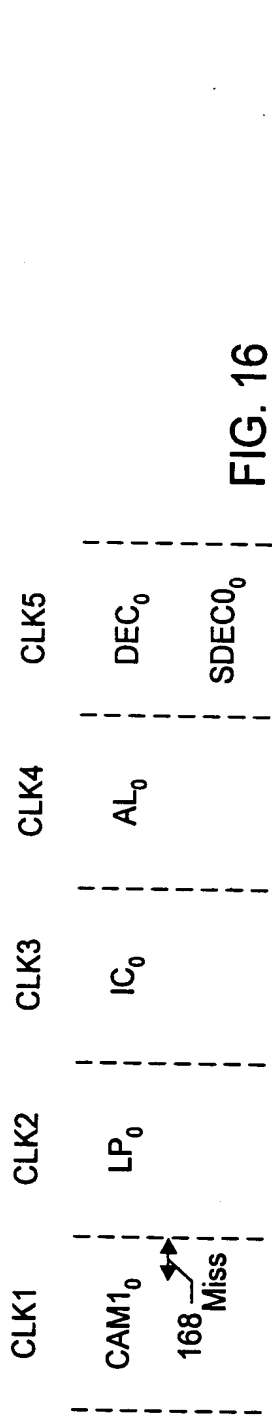


FIG. 15



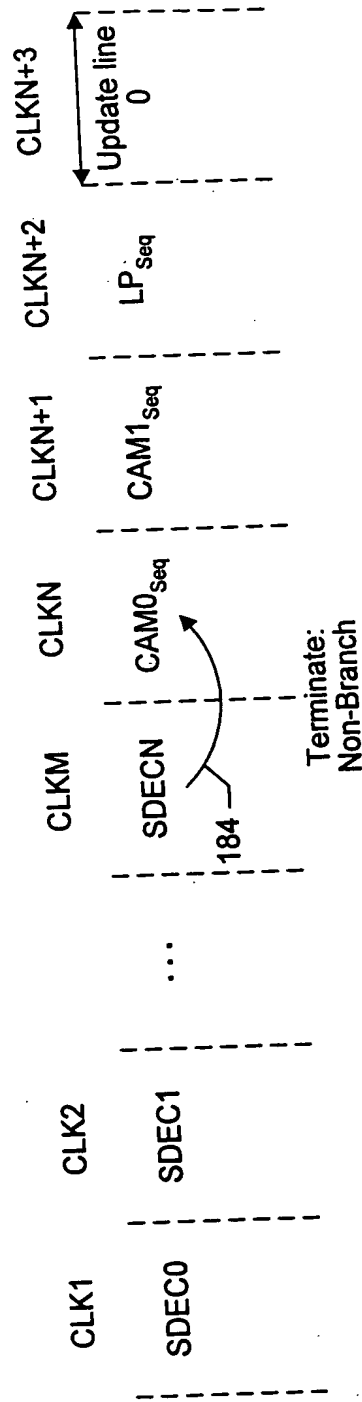


FIG. 19

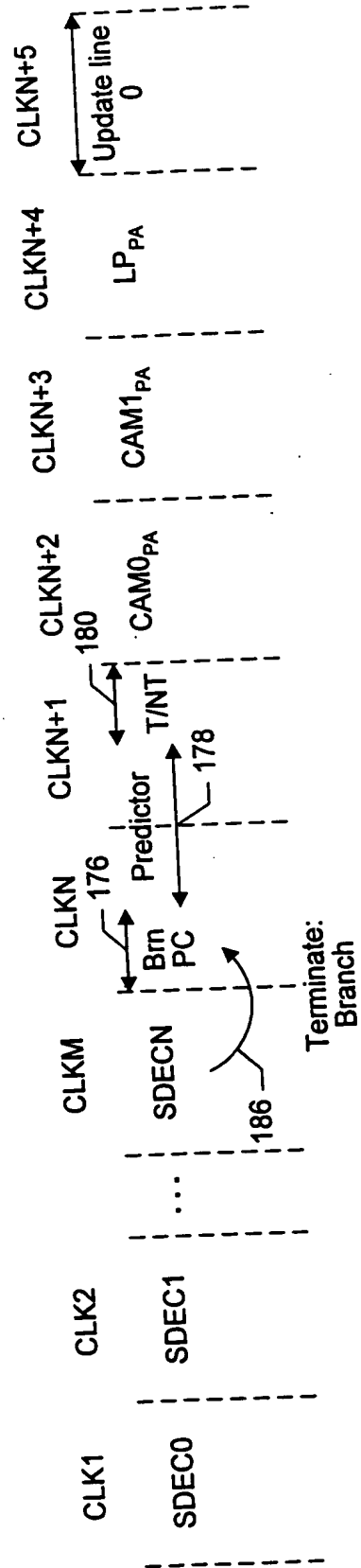


FIG. 20

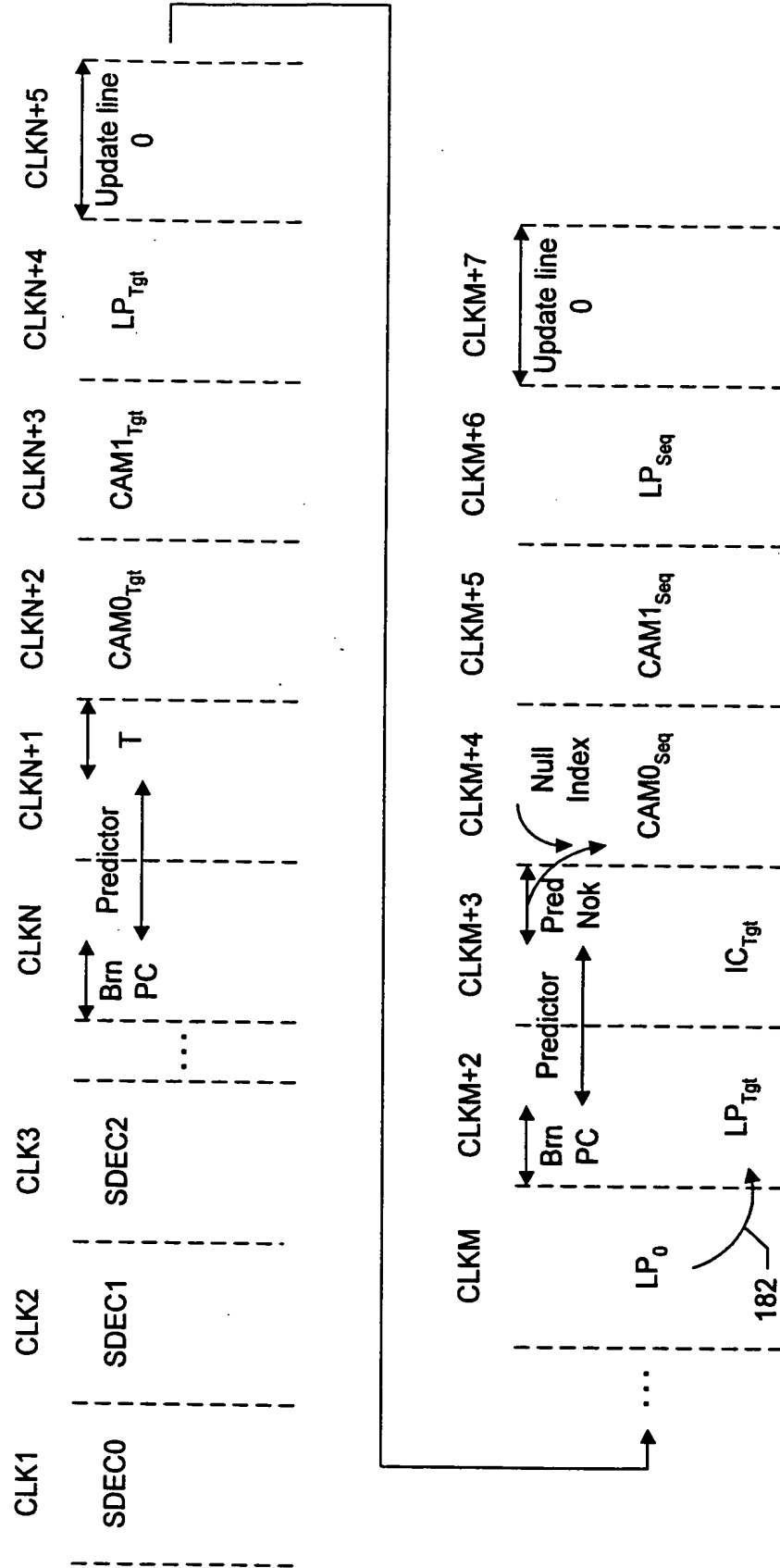


FIG. 21

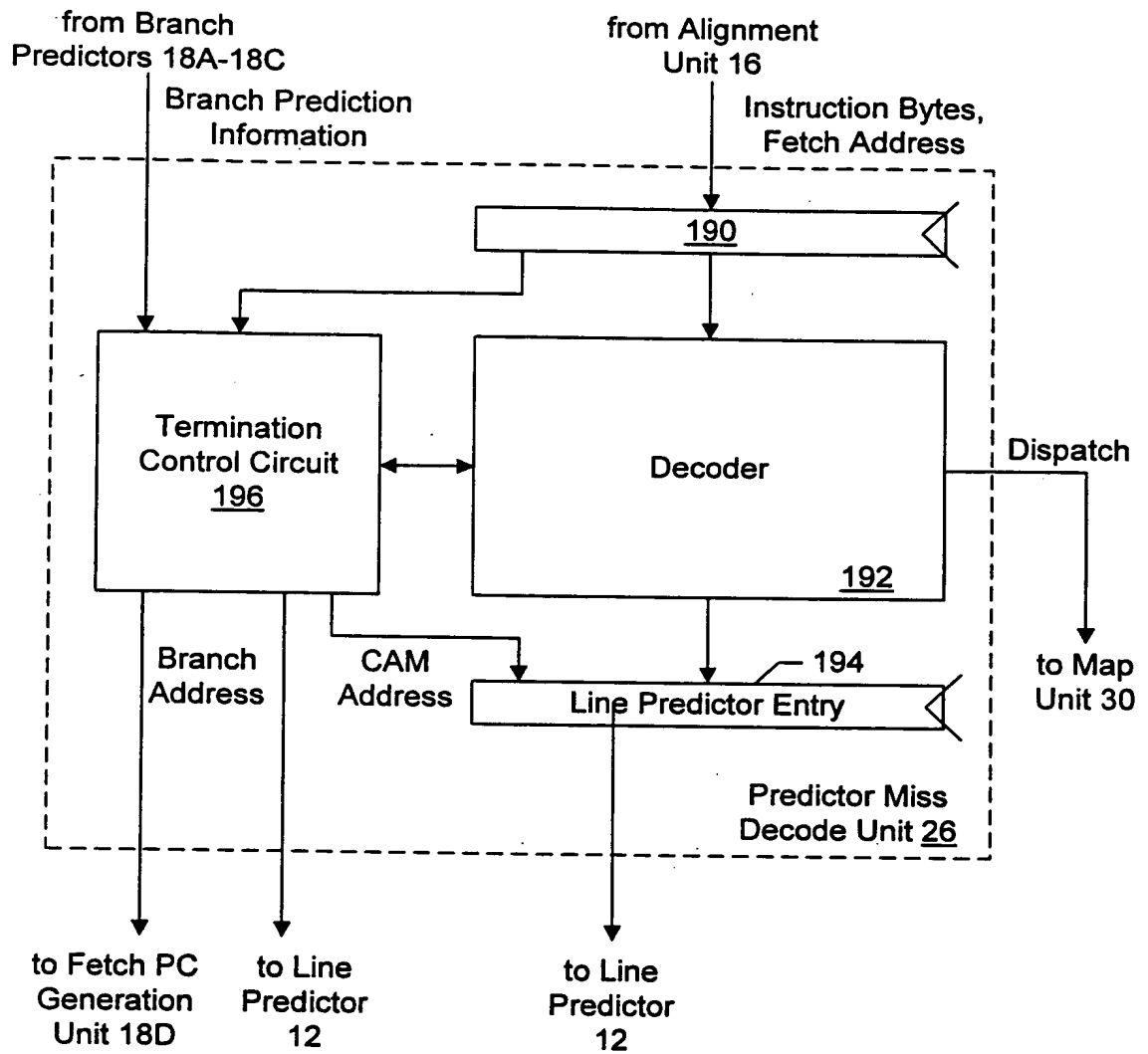


FIG. 22

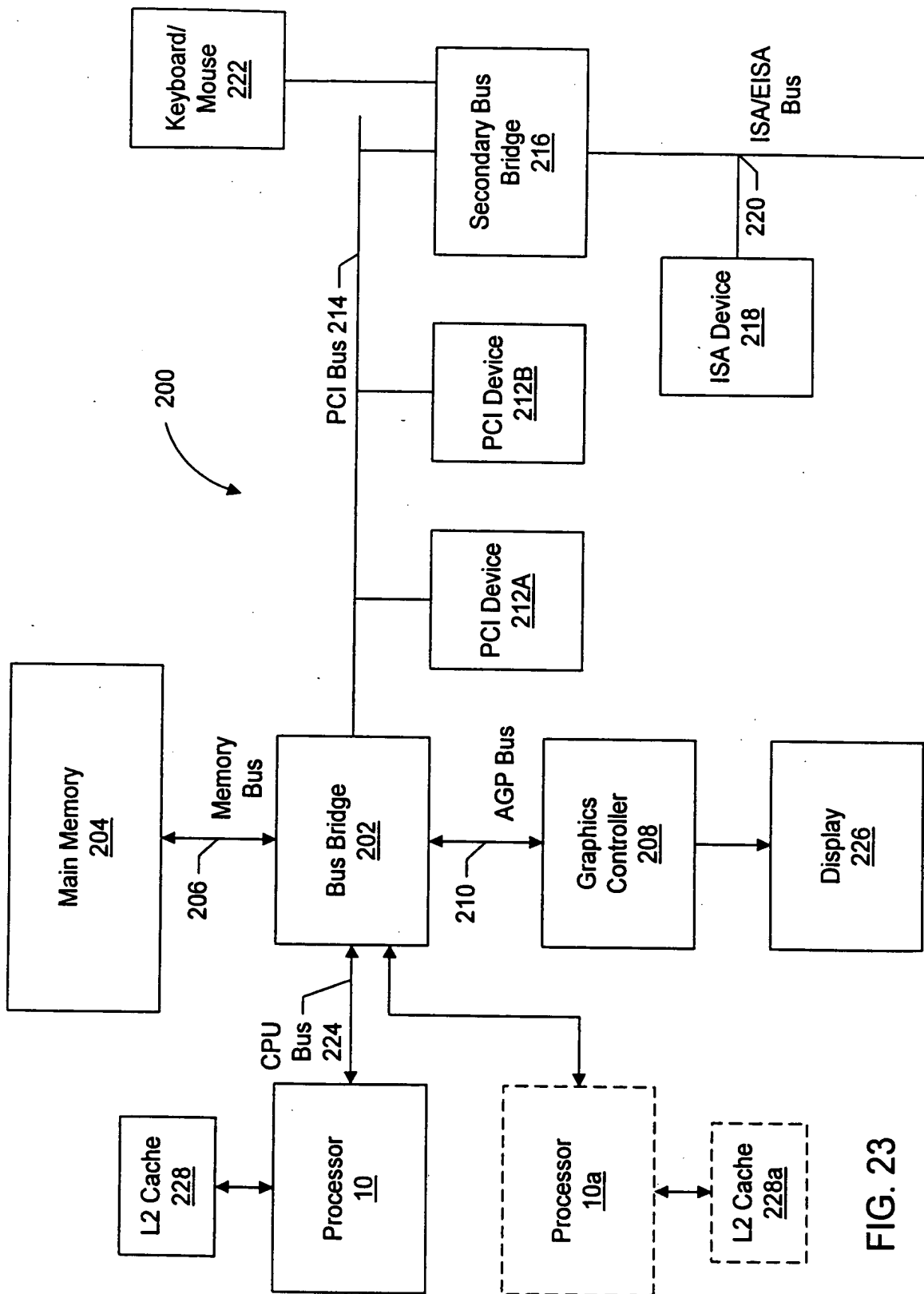


FIG. 23

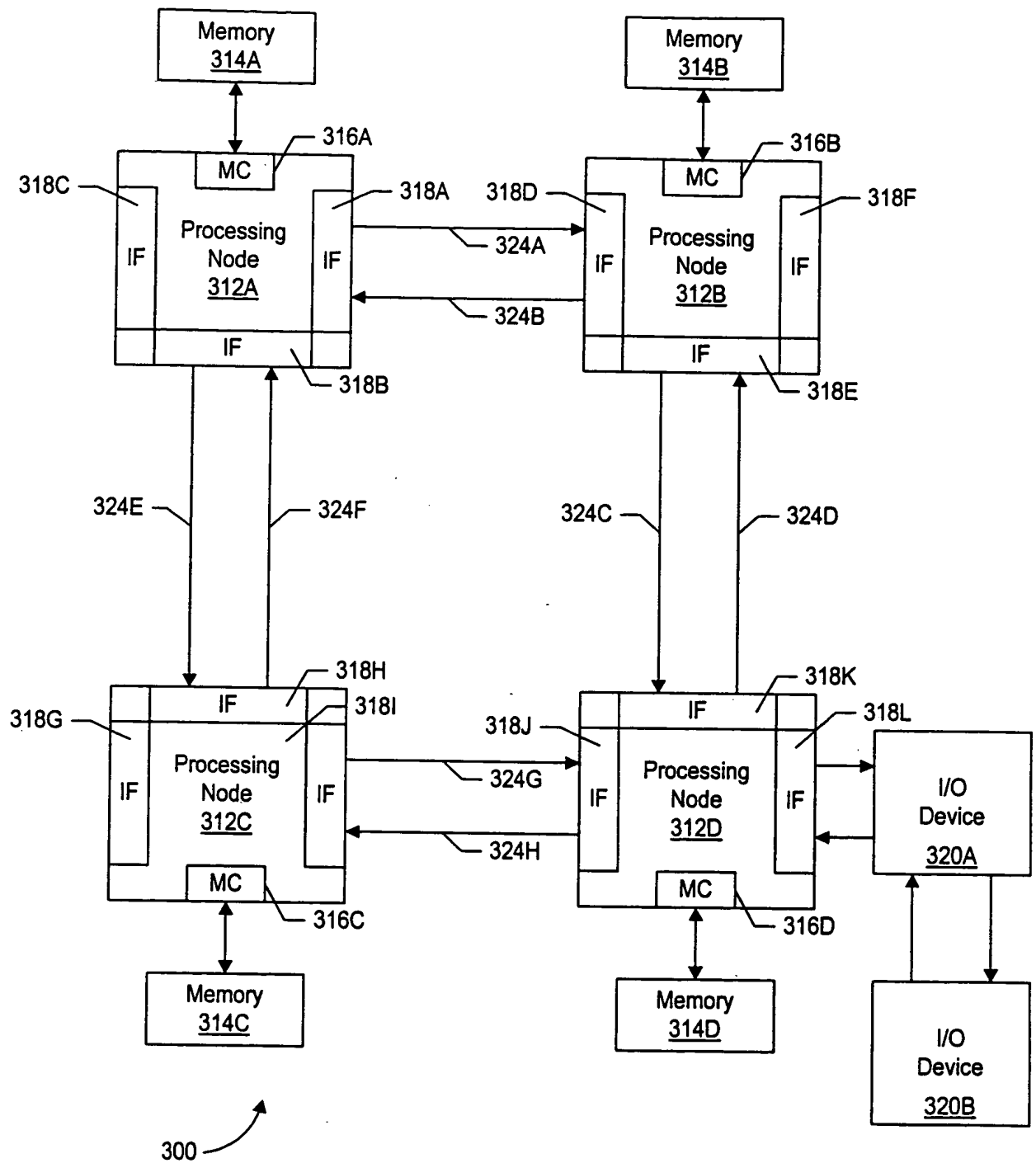


FIG. 24